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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/007,436	11/30/2001	Yan Chiew Chow	A-70117/ESW/WEN	3061

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EXAMINER	
RAYYAN, SUSAN F	

ART UNIT	PAPER NUMBER
2167	

DATE MAILED: 11/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/007,436	CHOW ET AL.	
	Examiner	Art Unit	
	Susan F. Rayyan	2167	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 November 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/25/02, 3/31/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-19 are pending.

2. Information Disclosure statements filed on March 25, 2002 and March 31, 2003 have been considered.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1,9,12-13,16-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Stallmo (US 5,708,769).

As per claim 1 Stallmo anticipates:

at least one memory matrix unit having a memory matrix capable of storing data therein at fig. 1, S1-S6;

and at least one management unit for interfacing between the memory matrix unit and the data processing system and being configured to reduce time for a program running on the data processing system to access data stored in the memory system by having at least one application programming interface (API) configured to store, manipulate, and retrieve data in the memory matrix based on a property of the data at fig.1, controller#3.

Stallmo teaches memory system for use with a data processing system comprising at least one memory matrix unit having a memory matrix capable of storing

data therein, and at least one management unit for interfacing between the memory matrix unit and the data processing system and being configured to reduce time for a program running on the data processing system to access data stored in the memory system by having at least one application programming interface (API) configured to store, manipulate, and retrieve data in the memory matrix based on a property of the data at fig.1, # S1-S6 and controller #3.

As per claim 9 same as claim arguments above and Stallmo anticipates: wherein the management unit and the memory matrix unit are configured to provide on-demand random access to data stored in the memory matrix at col.2, line 66, bridging to, col. 3, line7.

As per claim 12 Stallmo anticipates:

operating a memory system to accelerate execution of an application running on a data processing system, the memory system having a memory matrix unit with a memory matrix capable of storing data therein and a management unit configured to interface between the memory matrix unit and the data processing system fig.1, # S1-S6 and controller #3;

receiving data from the data processing system data, determining a property of the data, storing the data in a predetermined location in the memory matrix based on the property and retrieving the data from the memory matrix at summary, fig. 1,controller #3 and S1 –S6.

Stallmo teaches a method of operating a memory system to accelerate execution of an application running on a data processing system, the memory system having a memory matrix unit with a memory matrix capable of storing data therein and a management unit configured to interface between the memory matrix unit and the data processing system, comprising steps of receiving data from the data processing system data; determining a property of the data, storing the data in a predetermined location in the memory matrix based on the property and retrieving the data from the memory matrix at fig.1, # S1-S6 and controller #3.

As per claim 13 same as claim arguments above and Stallmo anticipates: the step of manipulating the data at col1, lines 15-22.

As per claim 16 same as claim arguments above and Stallmo anticipates: wherein the memory matrix comprises a plurality of Random Access Memory (RAM) devices arranged in a plurality of banks each having a predetermined number of memory devices at fig.1, # S1-S6;

and wherein the step of storing the data in a predetermined location in the memory matrix comprises the steps of: applying a row address and a column address to a port on at least one of the memory devices; latching the row address and the column address and applying the data to the port at col.4, lines 51-60.

As per claim 17 Stallmo anticipates:

wherein the step of retrieving data from the memory matrix comprises the step of providing on-demand random access to data stored anywhere in the memory matrix at col.2, line 66, bridging to, col. 3, line7.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 2-8,14-15,18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stallmo (US 5,708769) in view of Srivastava et al (US 6,549,922).

As per claim 2 same as claim arguments above and Stallmo does not explicitly teach wherein the memory system is compatible with Extensible Markup Language (XML) format structured documents, and wherein the management unit is configured to parse and store data from XML compliant documents according to data type, and to format XML documents into multiple presentation formats using Extensible Style sheet Language (XSL) templates however Srivastava does teach this limitation at col.2, lines 45-65. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the cited references to store data in a fashion that permits access to perform data management , search and retrieval at col.2, lines 1-7.

As per claim 3 same as claim arguments above and Srivastava teaches: wherein the memory system is capable of being synchronized with another XML enabled storage device at col.3, lines 50-62.

As per claim 4 same as claim arguments above and Srivastava teaches wherein the management unit is further configured to provide a running total of data having a specified property written to the memory matrix at col. 4, lines 51-60.

As per claim 5 same as claim arguments above and Stallmo does not explicitly teach wherein the property of the data includes a logical type of the data or an organization of the data however Srivastava does teach this limitation at col.4 lines 49-60. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the cited references to efficiently manage data.

As per claim 6 same as claim arguments above and Stallmo does not explicitly teach wherein the memory matrix comprises at least one component of a database, and wherein the memory system is SQL enabled to create, process, update, sort, and query the component of the database using SQL queries however Srivastava does teach this limitation at fig. 1 #125 and summary. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the cited references to perform data management in an efficient manner at col. 1, line 63, bridging to col. 2, line 6.

As per claim 7 same as claim arguments above and Srivastava teaches: wherein data in the database is stored as a plurality of records, and wherein the memory system is capable of compressing data stored in the database in real-time by recovering storage space of deleted records at fig.1, whereas prior art database deletes records and recovers storage space in a manner similar to the Applicant's claimed language.

As per claim 8 same as claim arguments above and Stallmo teaches: wherein the management unit is configured to provide custom partitioning, bit-level locking, and manipulation of data written to the memory matrix at summary and fig.1.

As per claim 14 same as claim arguments above and Stallmo does not explicitly teach wherein the step of determining a property of the data comprises the step of determining which one of a plurality of logical data types the data is, and wherein the step of manipulating the data comprises the step of providing a running total of data of a specific logical type and having a pre-specified criteria however Srivastava does teach this at col. 4, lines 51-60. It would have been obvious to one of ordinary skill in the art at the time of the invention to have combined the cited references to provide a means to perform advanced queries at col.5, lines 1-10.

As per claim 15 same as claim arguments above and Stallmo does not explicitly teach wherein the step of manipulating the data comprises the step of providing summary information about data of a specific logical type and having a pre-specified criteria however Srivastava does teach this at col.7, lines 48-55. It would have been obvious to one of ordinary skill in the art at the time of the invention to have combined the cited references to provide quick browsing of media at col. 7, lines 53-55.

As per claim 18 same as claim arguments above and Stallmo does not explicitly teach wherein the memory matrix comprises at least one component of a database having data stored as a plurality of records, the memory system being SQL enabled to create, process, update, sort, and query the component of a database using SQL queries, and wherein the steps of storing and retrieving data from the memory matrix

comprises the steps of storing and retrieving data from the memory matrix using SQL queries however Srivastava does teach this limitation at summary. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the cited references to manage data in an efficient manner at col. 1, line 63, bridging to col. 2, line 6.

As per claim 19 same as claim arguments above and Stallmo does not explicitly teach wherein the method comprises the further step of reclaiming storage space associated with a deleted record using SQL queries, whereby the component of a database is compacted in real-time however Srivastava does teach this limitation at fig.1, whereas prior art database deletes records and recovers storage space in a manner similar to the Applicant's claimed language. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the cited references to manage data storage in a manner which makes efficient use of available space.

7. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Stallmo (US 5,708769) in view of Srivastava et al (US 6,549,922) and further in view of Yao et al (US 6,021464).

As per claim 10 same as claim arguments above and Stallmo teaches:
wherein the memory matrix comprises: a plurality of Random Access Memory (RAM) devices each capable of storing data therein, the memory devices arranged in a plurality of banks each having a predetermined number of memory devices at fig. 1, S1-S6;
a memory controller coupled to each of the banks and capable of accessing the memory devices at fig. 1, controller#3;

a processor coupled to the memory controller of the banks of memory devices at fig. 2B;

a read-only memory (ROM) device coupled to the processor, the ROM device having stored therein an initial boot sequence to boot the memory matrix unit at fig. 2B;
a memory device coupled to the processor to provide a buffer memory to the processor at fig. 2B.

Stallmo does not teach a cache coupled to the memory controller, the cache having stored therein one or more copies of a file or Data Allocation Table (DAT) adapted to describe files data stored in the memory devices and a network interface controller adapted to couple the processor to a data network however Yao does teach these limitation at fig. 1 and fig. 1, #252 #252. It would have been obvious to one of ordinary skill in the art at the time of the invention to have combined the cited references to provide a means to effectively manage the actual location of files.

8. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Stallmo (US 5,708769) in view of Yao et al (US 6,021464).

As per claim 11 same as claim arguments above and Stallmo teaches:
wherein the management unit comprises: a primary processor coupled to the memory controller of the memory matrix at fig. 2B;
a read-only memory (ROM) device coupled to the primary processor, the ROM device having stored therein an initial boot sequence to boot the management unit at fig. 2B; and a memory device coupled to the primary processor to provide a buffer memory to the primary processor at fig. 2B.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Susan Rayyan whose telephone number is (703) 305-0311. The examiner can normally be reached M-F: 8am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Breene can be reached on 703-305-9790. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for Official communications, (703) 746-7238 for After Final communications and (703) 746-7240 for Status inquires and draft communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Susan Rayyan

October 27, 2004

Alford W. Kindred